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10/605,636	10/15/2003	Edward W. Lee	ML-15	2635

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EXAMINER
STIGLIC, RYAN M

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,636	LEE ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-12 and 14-20* is/are rejected.

7)☒ Claim(s) *4,5,13 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending and have been examined.

2. Claims 1-3, 6-12, and 14-20 are rejected.

3. Claims 4-5, 13, and 21 are objected to.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 6-7, 9-12, 14, and 17-20 rejected under 35 U.S.C. 102(b) as being anticipated by Pua et al. (US 20020147882A1).

Regarding claim 1, a chainable Universal-Serial-Bus (USB) flash-memory drive comprising:

- a drive substrate having wiring traces for electrically connecting components (Fig. 1A, 100; [0067]);
- a USB hub, mounted on the drive substrate, having a host port and a plurality of device ports (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]);
- a male USB connector mounted on the drive substrate, connected by the wiring traces to the USB hub (Fig. 1A, 10; [0067]);

- a female USB connector mounted on the drive substrate, connected by the wiring traces to the USB hub (Fig. 1A, 20; The substrate 100 contains a stack connector 20 for connecting a slave board to the substrate [0073]);
- a flash controller mounted on the drive substrate, connected by the wiring traces to one of the plurality of device ports of the USB hub (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]); and
- a flash memory mounted on the drive substrate, connected by the wiring traces to the flash controller, for storing data received by the USB hub through the host port (Fig. 1A, 50; [0067]),
- whereby the drive substrate has mounted thereon the male USB connector, the female USB connector, the USB hub, the flash controller, and the flash memory (Fig. 1A).

Regarding claim 2, the chainable USB flash-memory drive of claim 1 wherein the male USB connector connects to the host port of the USB hub; wherein the female USB connector connects to one of the plurality of device ports of the USB hub (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]).

Regarding claim 3, the chainable USB flash-memory drive of claim 2 wherein the female USB connector can connect to the male USB connector of a downstream chainable USB flash-

memory drive allowing a host connected to the male USB connector of the chainable USB flash-memory drive to read flash memory from either the chainable USB flash-memory drive or from the downstream chainable USB flash-memory drive, whereby the chainable USB flash-memory drive can be daisy-chained to the downstream chainable USB flash-memory drive [0073].

Regarding 6, the chainable USB flash-memory drive of claim 3 further comprising: a daughter-card that has a flash memory mounted thereon (Fig. 1B; [0073]); an expansion flash controller mounted on the drive substrate and connected to one of the plurality of device ports of the USB hub by the wiring traces (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as the expansion flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]); a socket on the drive substrate, the socket connected to the expansion flash controller by the wiring traces (Fig. 1A; item 20 on the right of substrate 100); secondary connectors on the daughter-card for fitting into the socket on the drive substrate (Fig. 1B; 110; [0073]), whereby expansion flash memory is mounted on the daughter-card but the expansion flash controller is mounted on the drive substrate.

Regarding 7, the chainable USB flash-memory drive of claim 6 wherein the secondary connectors on the daughter-card comprise metal contact pads along a long edge or along a short edge of the daughter-card, or comprise metal posts or a female connector plug (A connector such as item 110 of Fig. 1B inherently possesses conductive metal contact pads in order to transfer data between the substrate and the extension memory).

Regarding claim 9, the chainable USB flash-memory drive of claim 3 wherein the male USB connector and the female USB connector are mounted on opposite edges of the drive substrate (Fig. 1A).

Regarding claim 10, a daisy-chainable flash card comprising:

- a printed-circuit board (PCB) substrate (Fig. 1A; 100);
- a hub controller mounted on the PCB substrate, the hub controller having a host port, a first device port, and a second device port, the hub controller forwarding commands and data to and from the host port and the first device port or the second device port (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]);
- a male connector mounted on the PCB substrate and connected to the host port of the hub controller for insertion into a female connector on a host (Fig. 1A, 10; [0067]);
- a female connector mounted on the PCB substrate and connected to the first device port of the hub controller, for receiving a male connector on a downstream device (Fig. 1A, 50; [0067]);
- a flash controller connected to the second device port of the hub controller (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]); and

- a flash memory connected to the flash controller, for storing data from the host, wherein the hub controller routes data from the host to the flash controller for storage by the flash memory when the host addresses local flash memory, but the hub controller routes data from the host to the female connector when the host does not address the local flash memory (Fig. 1A, 50; [0067]; [0145]).

Regarding claim 11, the daisy-chainable flash card of claim 10 wherein the flash controller and the flash memory are chips mounted on the PCB substrate (Fig. 1A; [0067]).

Regarding 12, the daisy-chainable flash card of claim 10 wherein the flash controller is mounted on the PCB substrate (Fig. 1A, 40) but the flash memory is mounted on a daughter-card (Fig. 1B, 120); further comprising: a socket on the PCB substrate for receiving a connector on the daughter-card (Fig. 1A, item 20 "stack connector"; [0073]), wherein the flash memory connects to the flash controller through the connector and the socket.

Regarding claim 14, the daisy-chainable flash card of claim 10 wherein the male connector is a male USB connector, the female connector is a female USB connector, and the hub controller is a USB hub controller [0067-0073].

Regarding claim 17, an expandable flash card comprising:

- substrate means for physically supporting and electrically connecting components mounted thereon (Fig. 1A,. 100; [0067]);
- male protocol connector means, attached to the substrate means, for plugging into a female protocol connector on a host (Fig. 1A, 10);
- female protocol connector means, attached to the substrate means, for receiving a male protocol connector on a downstream device (Fig. 1A, 20; The substrate 100 contains a stack connector 20 for connecting a slave board to the substrate [0073]) ;
- protocol hub controller means, mounted on the substrate means, for routing protocol data from the host to an addressed port in a plurality of ports (The controller 40 of Fig. 1A (also Fig. 2, 200) serves as both the flash memory controller and a USB hub because it controls access to all memories on both the principle substrate and the daughter substrate; [0073-0079]);
- first memory means, mounted on the substrate means, for storing the protocol data from the host when the host addresses a port on the protocol hub controller means for the first memory means (Fig. 1A, 50; [0067]); and
- pass-through means for passing the protocol data from the host through to the female protocol connector means when the host addresses a port that is not in the plurality of ports of the protocol hub controller means, whereby protocol data is stored on the first memory means mounted on the substrate means, or is passed through from the male protocol connector means to the female protocol connector means ([0145]).

Regarding claim 18, the expandable flash card of claim 17 wherein: when a protocol is a USB protocol, the male protocol connector means is a male USB connector means, the female protocol connector means is a female USB connector means, the protocol hub controller means is a USB hub controller means, and the protocol data is USB data [0067-0073].

Regarding claim 19, the expandable flash card of claim 18 further comprising: socket means, connected to a second of the plurality of ports of the protocol hub controller means, for receiving a daughter-card containing a second flash memory means for storing the protocol data from the host when the host addresses a port on the protocol hub controller means for the second memory means (Fig. 1A, 20; The substrate 100 contains a stack connector 20 for connecting a slave board to the substrate [0073] thus providing unlimited memory expansion; [0145]).

Regarding claim 20, the expandable flash card of claim 18 wherein the protocol hub controller means further comprises address decode means for detecting and decoding protocol addresses received from the host over protocol data lines [0094-0103].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pua as applied to claim 3 above, and further in view of what was common knowledge to one of ordinary skill in the art at the time of applicant's invention.

As noted above with respect to claim 3, Pua teaches a chainable USB flash memory comprising a substrate (Fig. 1A) and a downstream expansion board (Fig. 1B). The substrate contains the necessary hub and controller functions to access the memories of the substrate and expansion modules. **OFFICIAL NOTICE** is taken that it was common knowledge at the time of applicant's invention to implement a PCB as a multi-layer PCB in order to provide more surface area for conductive wiring patterns as evidenced by Crepeau (US 4,249,302) (col. 2, ll. 37-54)..

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pua as applied to claim 10 above, and further in view of the IEEE Standard for a High Performance Serial Bus (i.e. IEEE1394 firewire).

As noted above with respect to claim 10, Pua teaches a chainable PCB USB flash memory comprising a substrate (Fig. 1A) and a downstream expansion board (Fig. 1B). The substrate contains the necessary hub and controller functions to access the memories of the substrate and expansion modules [0067-0073] along with the necessary connectors to attach the substrate to the host and the expansion memory modules. Pua however fails to teach the USB connectors (Fig. 1A, items 10 and 20) may also adhere to the IEEE-1394 firewire specification.

The firewire specification teaches of a high-speed, low cost serial bus connection that provides:

a) Automatic assignment of node addresses—no need for address switches.

b) Variable speed data transmission based on ISDN-compatible1 bit rates from 24.576 Mbit/s for TTL backplanes to 49.152 Mbit/s for BTL backplanes to 98.304 Mbit/s, 196.608 Mbit/s, and 393.216 Mbit/s for the cable medium.

c) The cable medium allows up to sixteen physical connections (cable hops), each up to 4.5 m, giving a total cable distance of 72 m between any two devices. Bus management recognizes smaller configurations to optimize performance.

d) Bus transactions that include both block and single quadlet reads and writes, as well as an "isochronous" mode that provides a low-overhead guaranteed bandwidth service.

e) A physical layer supporting both cable media and backplane buses.

f) A fair bus access mechanism that guarantees all nodes equal access. The backplane environment adds a priority mechanism, but one that ensures that nodes using the fair protocol are still guaranteed at least partial access.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the USB connections as IEEE1394 firewire connections since IEEE1394 firewire has the added advantage of architectural compatibility with parallel computer buses; this leads to lower communications overhead than limited function dedicated I/O interconnects

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as applied to claim 10 above, and further in view of Pua.

Applicant's admitted prior art (AAPA) teaches non-volatile flash memory is especially useful for small consumer devices such as digital cameras, music players, personal digital assistants, etc [0002]. Typically these flash memories are used to expand the storage capacity of a personal computer (or previously listed applications) [0003]. These flash memories adhere to several well known connection standards including secure-digital, memory-stick, or compact flash [0003]. However, applicant admits that one shortcoming of such flash memories is the limited capacity of internal flash memory chips [0006]. Applicant then admits that what is needed is an expandable flash-memory drive.

As noted above with respect to claim 10, Pua teaches an expandable flash-memory substrate (Fig. 1A, 100) that comprises a male connector (Fig. 1A, 10 or the item 20 on the left), a female connector (Fig. 1A, item 20 on the right), a flash memory controller, and a hub controller (Fig. 1A, 40; where the controller 40 serves as both the flash memory and a hub since the controller controls commands and data between the USB host and manages data in the flash memory [0069]). Pua also teaches that slave boards (Fig. 1B, 150) may be connected to the substrate **100** for extending the memory size of the substrate by the incorporation of additional flash chips (Fig. 1B, 120) [0073].

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the expandable flash memory of Pua into a standard flash memory as set

forth in AAPA (i.e. secure-digital, memory-stick, or compact flash) such that the user is provided with a flash memory having unlimited memory expansion (Pua; [00073]).

Allowable Subject Matter

10. Claims 4-5, 13, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The various cited prior art references pertain to memory cards and their use in expanding available memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS

PAUL R. MYERS
PRIMARY EXAMINER